REMARKS

Applicant notes with appreciation the allowance of claims 1-15, 33-47 and 65 and the finding that claims 16-17, 31-32 and 48-49 would be allowed if amended to overcome the rejections under 35 U.S.C. 112.

Rejection of claims under 35 U.S.C. § 112

Claims 16, 31, 48 and 63 have been amended in response to the rejections of paragraphs 2-3 of page 2 of the subject office action. In particular, Claims 16, 31, 48 and 63, rejected because the limitation "the supply voltage" lacks sufficient antecedent basis, have been corrected by deleting "the," in order to introduce the limitations without prior reference. With this amendment, the claims introduce no new matter; acceptance is respectfully requested.

Rejections under 35 U.S.C. §102(b) and §103(a)

Claims 18-30, 50-62 and 66 are rejected as being unpatentable over Franca-Neto et al (US Patent 6,507,915 B1) alone or in view of O'Sullivan et al (US patent 6,259,755 B1). Applicant respectfully traverses those rejections and requests reconsideration.

Base Claims 18, 50 and 66 are directed to a data transmitter or method that controls the rise or fall transition time of a data signal, where the rise or fall transition time is the time that it takes for the data signal to change from one state to the next. As illustrated in Figure 2, an input data signal din has very short transition times from low to high and from high to low. By contrast, the data signal dout has a substantially longer transition time t_r from low to high. Further, the transition time of the data signal is controlled to be proportional to the bit time of a bit clock. For example, see figure 6 described in the Specification from page 9, line 11. Figure 6 illustrates a circuit to control the voltage supply to a delay element such as that of Figure 5. This feedback circuit adjusts the control voltage, vctrl on line 151, so that the difference in delay between the delay elements 176, 177 is equal to one clock cycle, τ_{bit} (see Specification p. 10, lines 5-16). The control voltage also controls the overall delay of each delay element, such that decreasing the control voltage increases both the overall delay of both elements and the difference in delay between the elements. As a result, the timing and length of delay of each

delay element is a function of the bit time of the bit clock, t_{bit}. Summing these delays results in a single data output, which has a longer rise or fall transition time. Therefore, when the circuit of Figure 6 is used to control the delay elements, the resulting rise or fall transition time is proportional to the bit time of the bit clock.

Franca-Neto is directed to a circuit that separates clock and data signals. The circuit addresses problems that may occur in a system receiving asynchronous data signals. When such signals are sampled by a local clock, the system may incorrectly sample signals that occur at nearly the same time as the local clock. The circuit of Franco-Neto detects when the edge of a clock and data signal are nearly simultaneous, and responds by delaying the latter of the two signals (see Franca-Neto, Fig. 3, col. 4 lines 53-67 and col. 5 lines 1-4). This result is shown in the timing diagram of Figure 4, which illustrates the operation of the circuit of Figure 3. The input clock and data signals (elements 210 and 212 in Figure 4) are received at a time differential of 2 picoseconds, or S1 (see col. 5 lines 23-38). The output clock and data signals (elements 214 and 216) are separated by a greater time differential of 4 picoseconds, or S2. As a result of this separation, a system can accurately sample the data signal because the signal no longer occurs at the same time as a clock transition.

Applicant's system as recited in the rejected claims produces a data signal output, the rise or fall transition time of which is proportional to the bit time of a bit clock. This process is not taught or suggested by Franca-Neto. As explained above, rise or fall transition time is the time it takes for a signal to change from one state to another, such as from "high" to "low." The Examiner refers to a "high or low transition time control separator" in Franca-Neto; however, no such element exists. The Examiner cites element 110 of Figures 1, 3 and 5 in Franca-Neto, which is a clock and data separator circuit. This circuit adds a delay between two signals that are nearly simultaneous, so that the signals are no longer nearly simultaneous (see the timing diagram of figure 4). This delay merely separates the edges of the two signals, and a change in the rise or fall transition time of either signal is only incidental to this separation. There is no control of that incidental change in transition time, and the transition time is certainly not controlled to be proportional to bit time as claimed.

The Examiner further states that the separator circuit of Franca-Neto controls transition time to be proportional to bit time of the bit clock, referring to col. 5, lines 40-65. As explained

above, this circuit has no control over rise or fall transition time. Moreover, the cited paragraph explains how, in Franca-Neto, the clock and data signals each "controls" the other: when they are received simultaneously, the first signal (data or clock) causes the delay of the other. This delay is merely a delay in the onset of a signal, and does not change rise or fall transition time. In addition, the delay is not proportional to the bit time of the clock. In Franca-Neto the delay is triggered by the edges of the two signals, so a longer or shorter bit time of the clock has no effect on the delay, and certainly not on transition time.

The secondary reference O'Sullivan does not control transition time and thus does not overcome the shortcomings of Franca-Neto.

In summary, Franca-Neto does not teach Applicant's invention as claimed in Base Claims 18, 50 and 66. The signal separator circuit is distinct in form and function from Applicant's rise or fall transition time control. It does not exhibit control over the rise or fall transition time of any signal, nor does it suggest such control. Rather, it merely delays the onset of the second of two signals that occur simultaneously (see col. 4, lines 50-55). Franca-Neto teaches delaying one signal by the onset of another, but this control is unrelated to rise or fall transition time and is not proportional to bit time of a bit clock. Therefore, Applicant claims an invention that is distinct and nonobvious over the teachings of Franca-Neto, O'Sullivan and other prior art.

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CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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